THE BELL SYSTEM TECHNICAL JOURNAL
Vol. 61, No. 4, April 1982
Printed in U.S.A.

No. 10A Remote Switching System:

Peripheral Systems Architecture and Circuit Design

By J. M. ADRIAN, L. FREIMANIS, and R. G. SPARBER

(Manuscript received May 22, 1980)

This paper provides a general description of the circuits and units that make up the No. 10A Remote Switching System. The components of the system were designed to provide the operating and maintenance features of an electronic switching system, while keeping size, cost, and external equipment to a minimum. Fundamental new design approaches are described.

I. INTRODUCTION

The goal of this paper is to provide a general insight into the 10A RSS circuits and units making up the remote unit, with the exception of control which is covered in a separate article. These system building blocks are designed to provide the ESS features and maintenance desired while keeping size, cost, and external equipment to a minimum. Fundamental new design approaches important to obtaining these goals were pursued and are emphasized when encountered in the following sections.

II. LINE INTERFACE

Switching systems with metallic networks, such as ESS No. 1, 2, and 3 provide the battery feed and rotary dial digit collection functions on a concentrated basis. The architecture of the RSS and the nature of its network require a circuit incorporating these functions at each line appearance (see Fig. 1). It is the purpose of the line interface to implement those functions efficiently and economically.

The major problem with adapting a conventional battery feed ar-

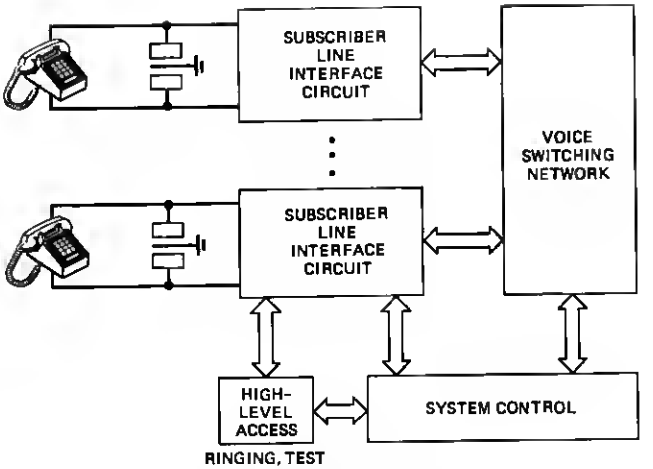


Fig. 1—RSS line interface.

rangement for RSS is heat dissipation. Eight such circuits feeding short loops may dissipate over 30 watts and, if densely packaged, require elaborate cooling facilities. Another requirement unique for RSS line interface is protection of the rather fragile network from hostile outside plant interferences, such as lightning and power crosses. Furthermore, the supervisory functions must be performed in face of substantial 60-Hz longitudinal induction.

The line interface circuit developed for RSS dissipates no more than 650 mW, and because of its floating nature is immune to longitudinal interference. Lightning protection for the network is provided by an isolating voice frequency transformer, voltage limiting semiconductors, and the junctor structure of the network itself.

The dramatic reduction (see Fig. 2) of heat dissipation is achieved by using a compliant floating power converter. The converter has three modes of operation. In the full-power mode, it supplies controlled current to the microphone and *TOUCH-TONE** service oscillators, collects rotary dial pulses, and supervises switch hook signaling, and generates a voltage proportional to loop resistance used for transmission compensation. The maximum current supplied on zero loop is based on a comprehensive study of the effect of loop current on transmission/grade of service (Ref. 1), and the converter maintains this current when the battery voltage drops during commercial power failure. Most of the time, however, the subscriber's station is on-hook, and the system is waiting for a service request. To conserve energy

* Registered service mark of AT&T.

	CONVENTIONAL 2 x 200 Ω	CONVERTER
MAXIMUM LOOP LENGTH 48 V BATTERY	1800 Ω	1600 Ω
WORST-CASE HEAT DISSIPATION	4.2 W	0.85 W
AVERAGE BATTERY POWER	2.3 W	1.4 W
LOOP CURRENT RANGE	100-23 mA	42-23 mA
ORIGINATION MODE POWER	0	50 mW

Fig. 2—Performance comparisons between conventional battery feed and RSS line interface.

and reduce heat dissipation, the converter is put into a low-power origination mode consuming only about 50 mW.

During ringing and loop testing, the audio and battery feed must be disconnected from the loop. This is accomplished by stopping the converter and allowing the disconnect thyristor to open (Fig. 3). Twenty-Hz ringing is then applied from a common bus via dry reed relay contacts. There are two such relays for each line interface circuit to accommodate ringing in the busy hour, as well as line testing. The relays are controlled by the system via latches and relay drivers on a per-line integrated circuit. This integrated circuit (IC) also controls the

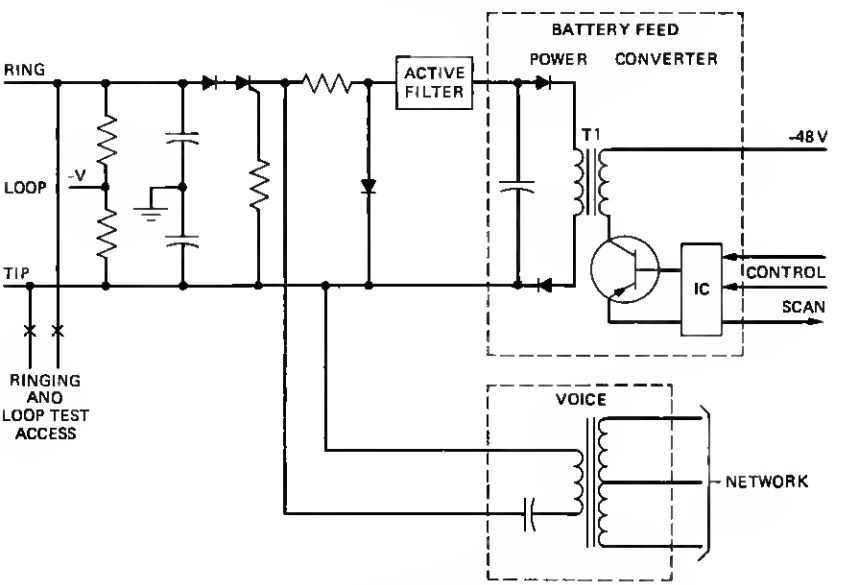


Fig. 3—Functional schematic of RSS line interface circuit.

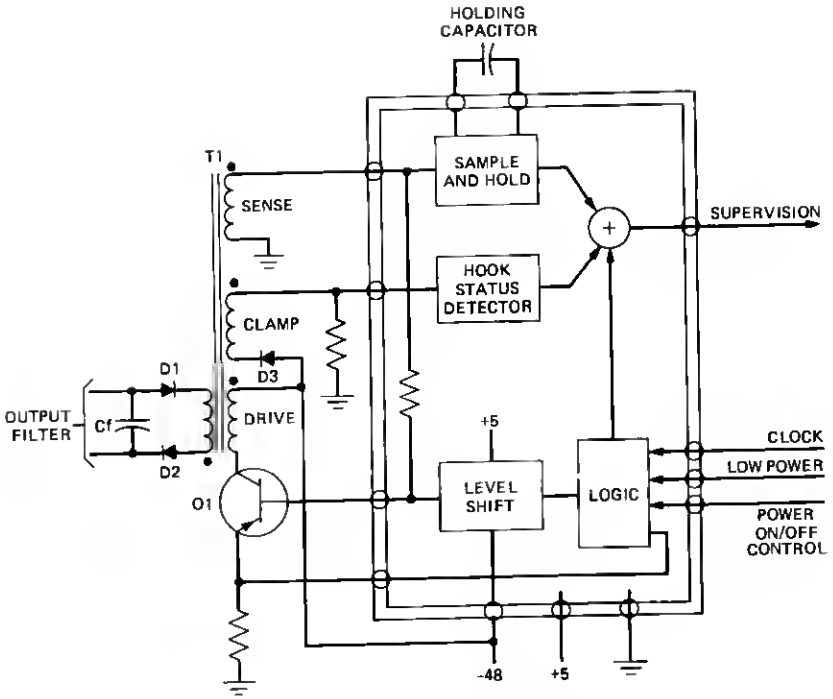


Fig. 4—Block diagram of the converter IC.

states of the converter, participates in the network path set up, and multiplexes the supervisory information onto the data bus.

Another integrated circuit (Fig. 4) controls the switching transistor in the power converter. In the full power mode with the switching transistor on, a linear current ramp is generated in the drive winding and energy stored in the magnetic field of the pulse transformer. Output rectifier diodes are reverse-biased, and base drive to the switching transistor is supplied by the sense winding. The ramp is terminated at a predetermined level by the comparator via a level shift circuit. Voltages on all windings reverse and the stored energy discharges into the filter capacitor and the loop. When the discharge is complete, voltages reverse again and the negative swing on the sense winding initiates a new cycle.

An equilibrium condition is imposed by the equal voltage-time product requirement on the output winding, and establishes an average voltage on the filter capacitor unique to the loop resistance. A scaled version of this voltage is sampled on the sense winding and held on the holding capacitor. An appropriate fraction of this voltage is applied to the scan point and multiplexed to the data bus.

In the full power mode, the converter frequency becomes a function of the loop resistance and varies between 40 and 90 kHz.

When the loop resistance increases above 2000 ohms, the positive and negative voltage excursions on the output winding become equal in amplitude, and the converter enters into a clamp mode. Excess energy is returned to the battery during the discharge cycle, and the peaks of the return current pulses are sampled by a comparator, which triggers a timer and activates a pull-up current source on the scan point whenever the loop resistance is above 7000 ohms, indicating a break in the rotary dial pulse or a switchhook signal. In the low-power origination mode, current has to be supplied only to loop leakages and the control of the converter is transferred to a low-frequency clock. Power dissipation is further reduced by disabling part of the level shift circuit between clock pulses. Negative bias for the level shift circuit is derived from the −48 volt battery by an on-chip isolated zener diode string. The pull-up source in this mode is kept active by the voltage on the hold capacitor. When service is requested by closing the loop, this voltage drops, trips the comparator and deactivates the source. The supervisory trip point in this case is considerably higher than in the full power mode (see Fig. 5). This feature eliminates the need for a pretrip test before 20-Hz ringing is applied. Ring-trip supervision during the silent intervals will be performed by the line circuit in the full power mode with reduced sensitivity to loop leakages.

The presently used line interface circuit in RSS (see Fig. 6) has been designed for a maximum loop resistance of 1600 ohms. An extended range can be readily accommodated by adjusting the turns ratio on the pulse transformer.

III. VOICE NETWORK

The main switch in the remote switching system is the voice network. It is an electronic space division network using PNPN semiconductor crosspoints for two-wire balanced audio transmission. Thirty-two PNPN crosspoints are fabricated on an integrated circuit. The network is formed from these PNPN ICs interconnected with a junctor circuit at the center feeding bias current to maintain active network paths. Specialized integrated circuits have been developed for network terminal control and to form the junctor circuit. Several alternative network technologies, including time division, were considered for RSS during its design. None was found superior to the design presented here with respect to size, cost, growth characteristics, or power.

3.1 The PNPN

A PNPN is a silicon device consisting of four alternate *p*- and *n*-semiconductor regions. A more common name, usually applied to

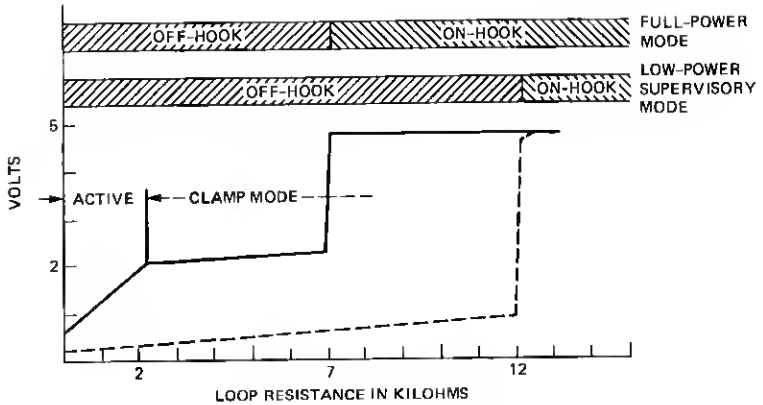


Fig. 5—Voltage levels on scan point.

higher power devices, is the silicon controlled rectifier or SCR. Two transistors may be interconnected as in Fig. 7 to simulate the device. For use in RSS, a series gate diode to simplify control and an anode-to-gate resistor to reduce transient turn-on susceptibility are added. Like an SCR, if current is drawn anode-to-gate, while current is flowing anode-to-cathode, the gate current may be removed and the PNPN will continue to conduct anode-to-cathode. Since no other state storage device is used, this effect is called self-latching. Thirty-two PNPN elements—the PNPN, gate diode, and anode-to-gate resistor—are formed on a common integrated circuit[2] in a 4 by 8 array shown in Fig.

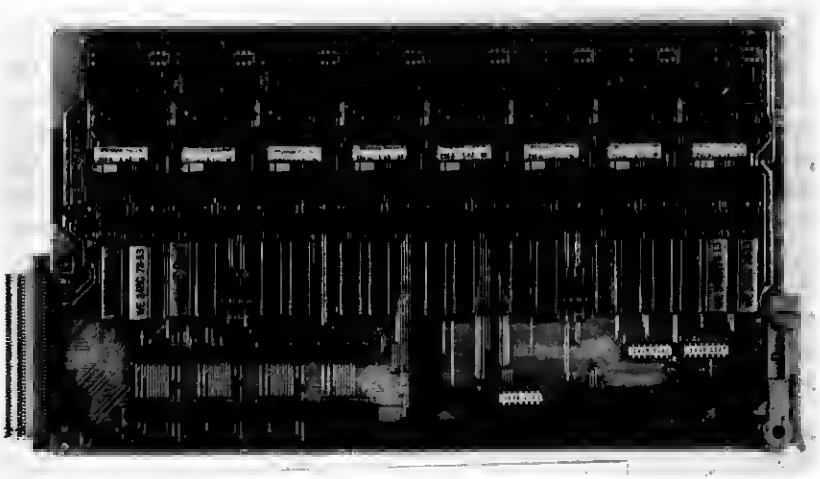


Fig. 6—FE101 line interface circuit pack.

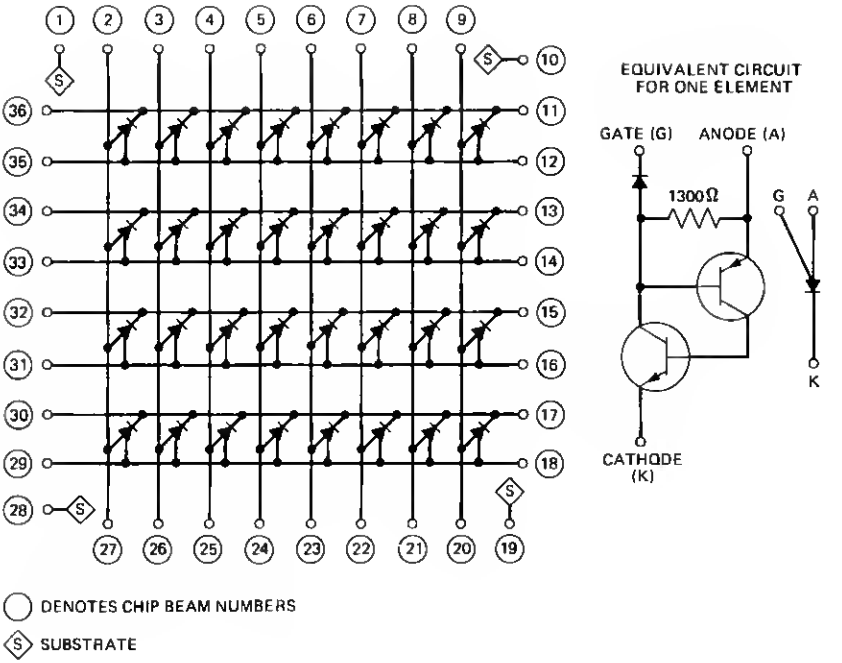


Fig. 7—Equivalent circuit of the PNPN array.

7. The conductor common to eight-gate diodes is called the diode rail. Table I shows the RSS PNPN to have reasonable on-resistance and off-capacitance parameters. This corresponds to low loss and crosstalk. This PNPN was also designed to have very low ac signal-to-substrate

Table I—Electrical properties of the PNPN array

Characteristics and Conditions	Typical (T = 25°C)	Units
DC Cathode-substrate leakage current (Iak = 0, Vak = 35 V)	0.6	μA dc
AC Cathode-substrate leakage current (Iak = 10 mA dc, Iak = 10 mA peak-to-peak, Vas = 20 Vdc)	0.03	μA pp
Forward leakage (Vak = 30 Vdc, Vks = 0 V)	0.01	μA dc
Reverse leakage (Vak = 30 Vdc, Vks = 0 Vdc)	0.01	μA dc
Gate-anode leakage current (Vag = 30 Vdc, Vas = 0 V)	0.01	μA dc
On-resistance (Iak = 10 mA dc)	9.0	Ω
Forward voltage (Iak = 10 mA dc)	0.9	Vdc
Holding current	1.1	mA dc
DC gate trigger voltage (Vak = 20 Vdc)	1.35	Vdc
DC gate trigger current (Vak = 20 Vdc)	0.6	mA dc
Anode-to-cathode capacitance (Vak = 20 V)	1.0	pF

Iak = Current anode-to-cathode
Vak = Voltage anode-to-cathode
Vas = Voltage anode-to-substrate
Vks = Voltage cathode-to-substrate
Vag = Voltage anode-to-gate

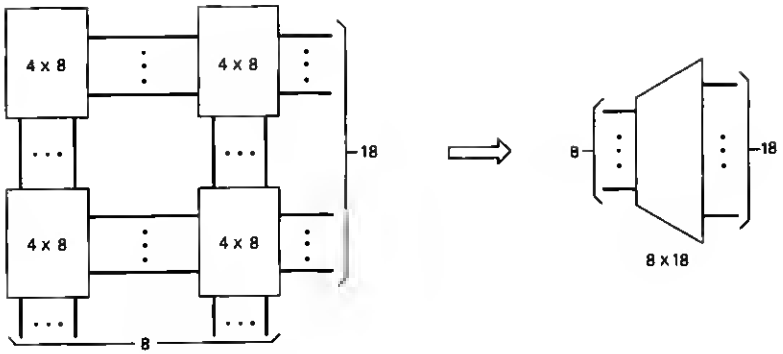


Fig. 8—Construction of line interface pack 8 x 16 switch.

loss—a common problem in this type of device—to keep loss variation negligible.

3.2 Topology, partitioning, and growth

The RSS voice network topology is quite rich especially in the first stage with 68 percent of the total crosspoints. This is possible because of the low cost and small size of the PNPN crosspoint used, but is enhanced by a network partitioning that allows the first stage to be equipped only as needed. Good traffic handling capabilities have resulted while rearrangement of line appearances, because of the possibility of high traffic lines tying up a first-stage switch, have been minimized.

Each line interface pack, LI, in RSS has an 8 by 16 expansion stage made from the 4 by 8 PNPN ICs, Fig. 8. Two-wire balanced transmission

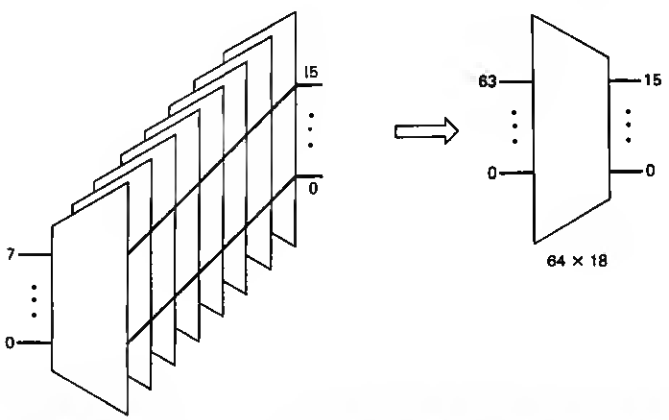


Fig. 9—Construction of 64 x 16 first-stage switch using multiple line interface pack 8 x 16 switches.

is used in the network so each lead shown is physically a pair of wires and each 4 by 8 switch is actually two 4 by 8 PNPN ICs. The network leads between the first and the second stage are called links. A full 64 by 16 first-stage line concentrator is formed by parallel connections of the links of 8 LI pack 8 by 16 switches, which are physically adjacent, as shown in Fig. 9. Carrier interface, (CI) packs use a similar arrangement of four 4 by 16 switches to form a 16 by 16 switch.

A full 512-line RSS network with two-stage folded topology is shown in Fig. 10. The first stage is made up of the CI, LI, and receiver off-hook (ROH) packs with the second stage formed from the 16 by 16 switches on the grid-junctor (G-J) pack. *TOUCH-TONE* service packs are not

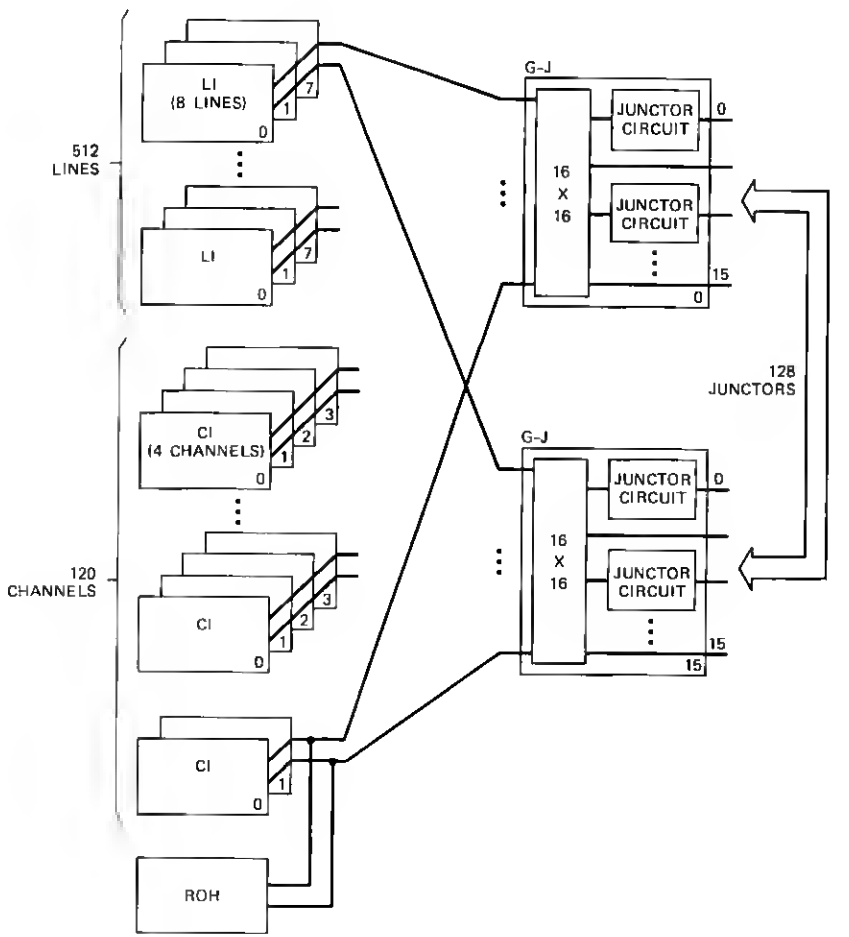


Fig. 10—Network configuration for up to 518 lines.

shown, but multiple onto the last CI switches. A path through the network is folded in that it always passes through a first-stage switch, a second-stage switch, a junctor circuit to bias the path, then back through a second-stage and first-stage switch. A complete junctor circuit is on each even appearance of the 16 by 16 second-stage switch, while odd appearances have no junctor circuit. The interconnection of the 16 by 16 switches is by leads, called junctors, that always connect an even switch appearance to an odd, including one complete junctor circuit in each junctor.

Growth of the network beyond 512 lines requires use of Build-Out Switch (BOS) packs that enlarge the second-stage switches from 16 by 16 to 24 by 24 and include extra junctor circuits on all even junctor

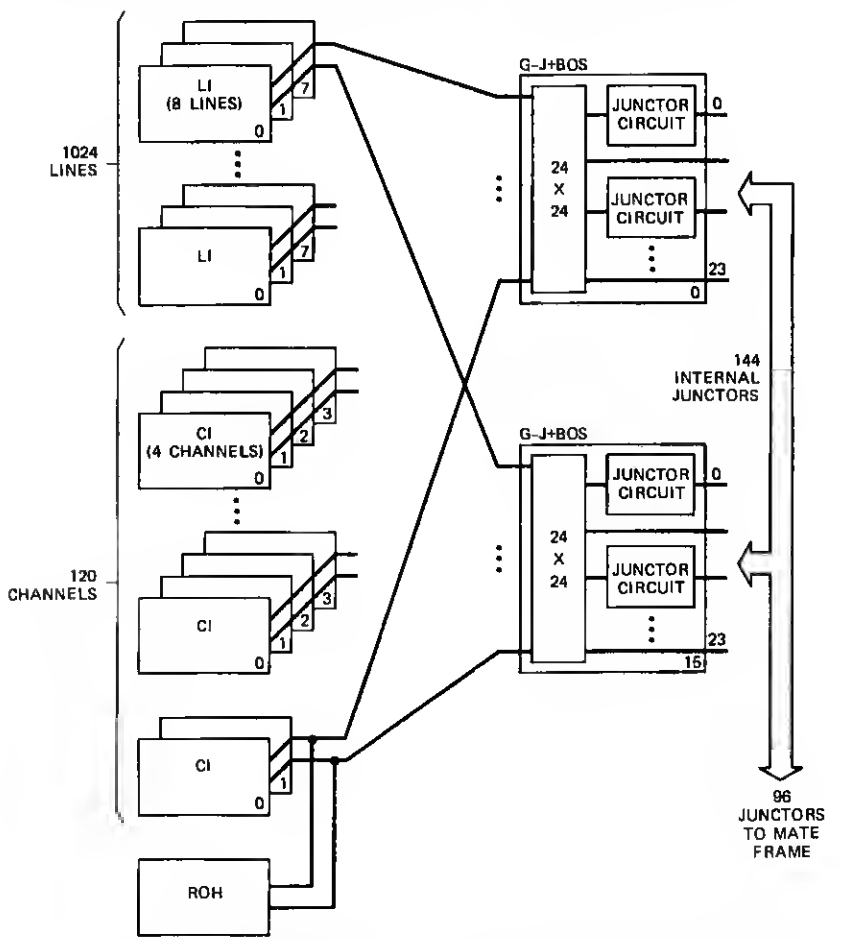


Fig. 11—Network configuration for up to 1024 lines and interconnect to optional mate frame.

appearances, as shown in Fig. 11. This expansion allows growth to a full single mod frame capacity of 1024 lines and extra junctors to interconnect to a 1024-line RSS mate frame with an identical network yielding a network growth limit of 2048 lines.

The RSS network traffic limit for the line-to-line calls is shown in Fig. 12 for a single frame. This curve assumes deloading line appearances by not equipping all 64 lines in a line concentrator to gain extra traffic capacity.

3.3 A PNPN voice network path

A line-to-line network path is shown in Fig. 13. In an active stable path, all current sources in the used junctor circuit are on with current from them passing through the on or active PNPNs to be sunk by the line-audio coupling transformer center taps. Many PNPNs are not shown that connect from this active path to other lines, but they are all off. The diode rails from the used PNPNs are at a high potential such that no gate current is sunk. The PNPNs in the active path are held on or latched only by the current bias from the junctor circuit. At least the current from one hold current source (I_{HA} or I_{HB}) will always flow through each PNPN in the path because of the diodes in the junctor circuit. A pair of coupling capacitors in the junctor circuit center allows for small dc voltage offsets in the path.

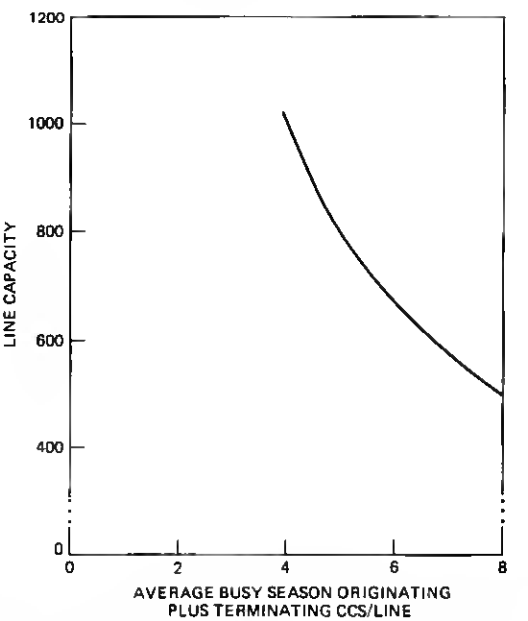


Fig. 12—Remote switching system line capacity—one-module RSS.

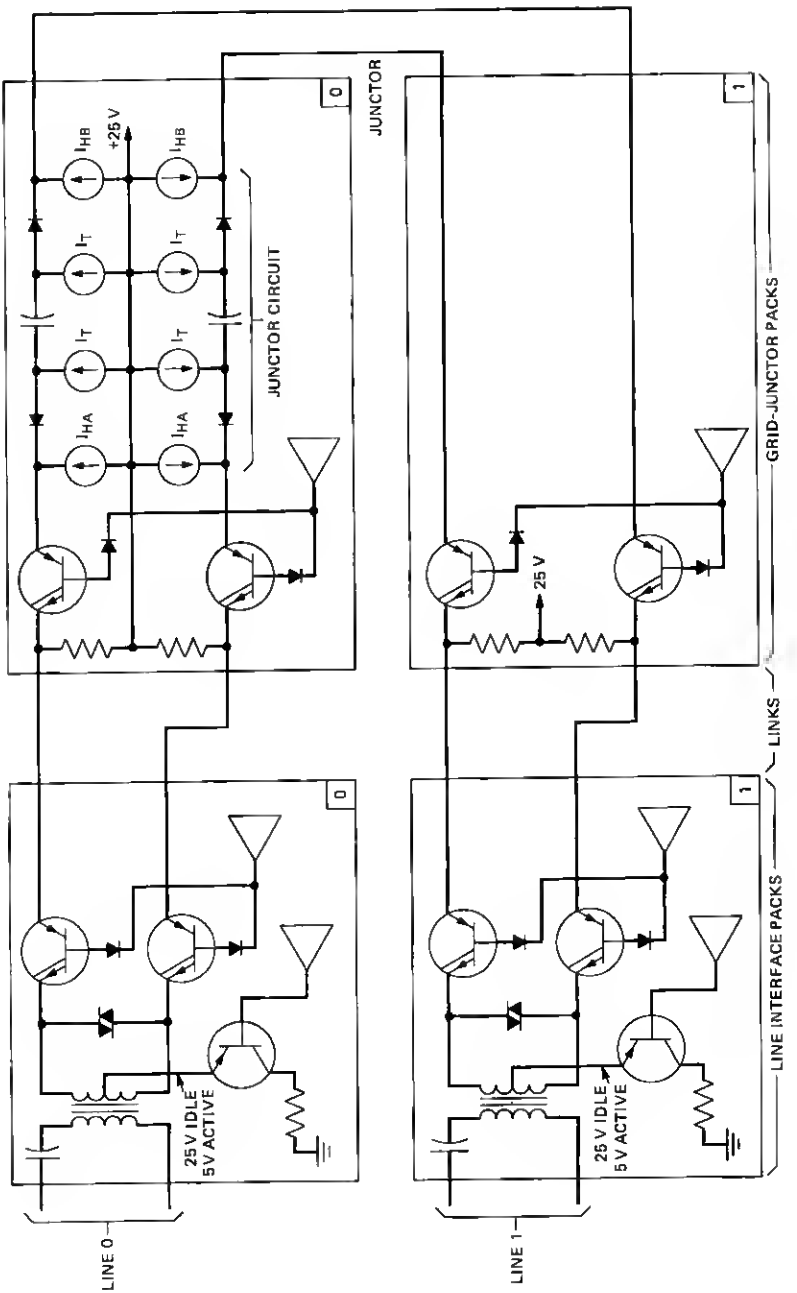


Fig. 13—A line-to-line network pass.

Path setup starts at the junctor circuit where the hold and talk sources are controlled as three separate groups: I_{HA}, I_{HB}, and I_T. Initially, all points in an idle path are at a high potential and all junctor circuit current sources are off. The path is set up in halves working from the junctor circuit. Starting, I_{HA} is enabled, the two diode rails are sequentially operated to their lower potential, and then the audio coupling transformer center-tap is lowered on line 0. The operated diode rails are now released. Repeating the process from I_{HB} through G-J pack 0 to line 1, two half paths are constructed. Finally, the talk sources, I_T, are enabled to complete the audio connection. Since the path potential is now controlled by the center-tap 5-volt potential, other paths may be constructed without interference with this path. All diode rail and center tap control potentials are ramped to eliminate parasitic coupling between paths momentarily canceling active path current and dropping paths.

To release a network path connection, talk sources are disabled, transformer center-taps are brought back to a high potential, and hold sources are disabled.

3.4 Network support circuitry

Associated with the network path is the control, current bias, and maintenance circuitry. In RSS, this circuitry has been integrated where practical. Check circuitry is included to detect faults and localize them.

At the network terminals—a line, channel, or other network point, a special bipolar IC is used incorporating a form of I^2L logic and analog interfaces.[3,4] This IC has many functions as discussed in Section II; however, here its important capabilities are controlling the 25-volt potentials of the voice network center-tap and diode-rail of a network terminal. Also, this IC repeats the bias current from the center-tap through a resistor and can repeat the developed potential to the fanout pack. This point is examined for no bias before path construction is initiated, after the center-tap is brought low for hold bias, and before a path is torn down for hold, plus talk bias.

The junctor circuit of RSS is made with a special bipolar IC also. Two of these ICs, plus two capacitors make up each junctor circuit exclusive of control. This IC, shown in simplified form in Fig. 14, contains the hold sources, talk sources, and diodes. A hold scan point is included which indicates three states: hold source off; hold source on and supplying current; and hold source on and not supplying current. The talk current sources are modified to appear as an ideal current source with a negative resistance to ground. This negative resistance cancels some of the line circuit and network losses to yield a typical 0.5-dB loss line-to-line.

Each G-J and BOS pack also contains control logic and diode rail

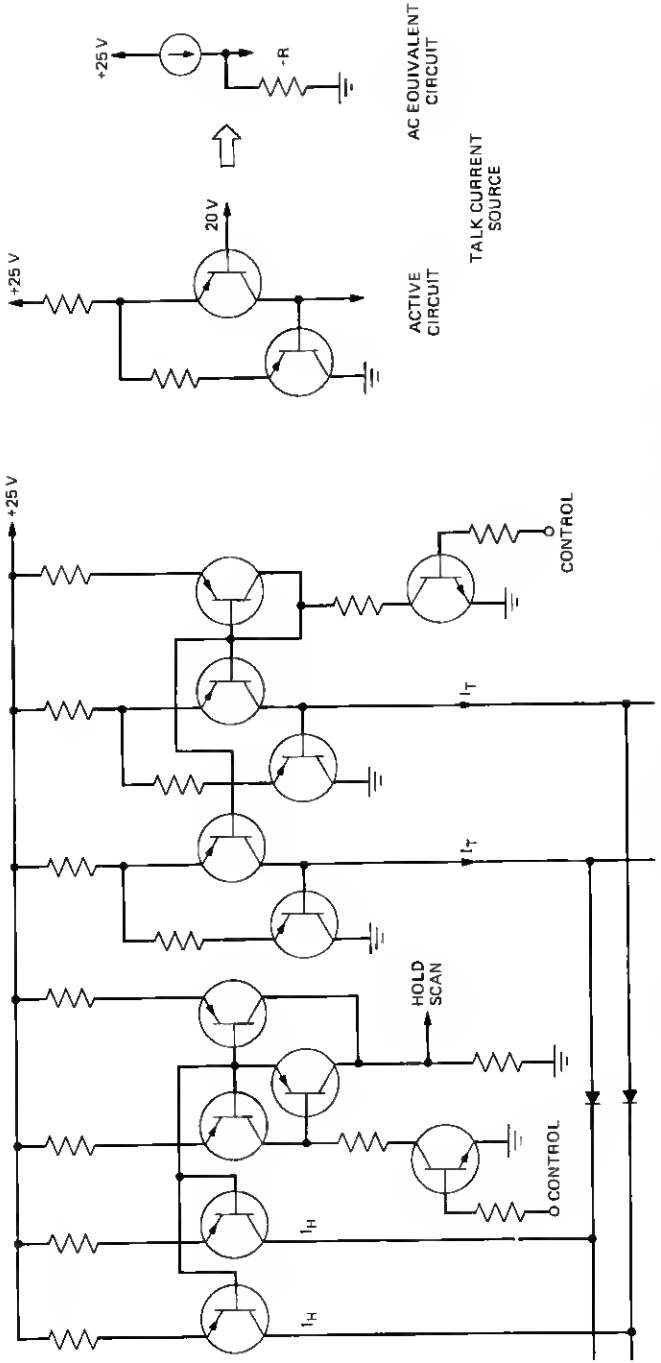


Fig. 14—Junctor circuit diagram and implementation of negative resistance.

drivers. The latches that contain the state of the diode rail driver and talk sources may be read back to the fanout pack. Circuitry to guard against system malfunctions clears any diode rail after 100 ms and will not allow the hold B sources to be enabled before the hold A sources.

IV. UNIVERSAL SERVICE CIRCUIT OVERVIEW

The Universal Service Circuit (USC) performs customer line functions which cannot be performed through the ac-coupled low-power electronic network of RSS. Figure 15 shows a photo of the USC which is, in essence, a 15-watt dc-dc converter with current sense on its outputs. It can supply ringing, coin control, party test, and test for power cross on a line among other functions. Each line circuit in RSS has two metallic reed relays which connect to a group of four USC packs which contain a second stage of switching.

The USC combines functions which have been performed by a number of separate circuits in previous ESS systems. Also, the USC, and its associated metallic connection to a line, is only used during the actual high-power interval of the line function—for instance, when ringing is applied, but not during the silent interval between rings. This combination of functions and time-divided usage allows for far fewer USCs than would be required using more dedicated circuits and a reduction in high-level network size. The high-level network is also used to gain metallic access to the line through the USC for several low-occupancy test circuits.

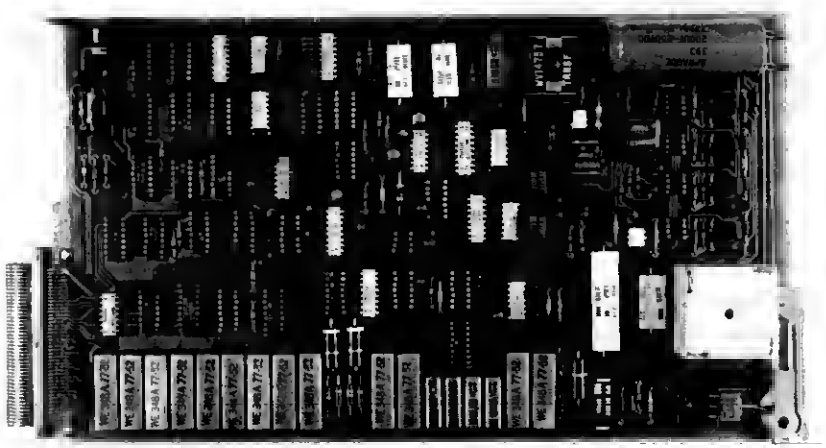


Fig. 15—Universal-level service circuit circuit pack.

4.1 Universal servica circuit dascription

Figure 16 is a functional representation of the USC pack. The USC supplies dc output voltages of ±150 volts in increments of 10 volts from a switching mode amplifier voltage source under control of a fanout pack. The current is limited to ±125 mA from the amplifier by an optically coupled overcurrent sensing circuit. This protection is provided for both directions of current. The ac ringing voltage of 88 volt rms 20 Hz may be superimposed on any selected dc output voltage up to ±80 volts. The amplified voltage is then applied to one of the eight possible high-level metallic access buses through selectable output impedances of 200 ohms, 2 kilohms, or 20 kilohms. Voltage and ground may be applied on either tip or ring. Two test-access ports are also available for those test circuits that require metallic access to lines.

The USC packs can also measure voltages to ±200 volts and currents to ±80 mA. Voltage is directly fed as a fraction of the voltage present to the fanout pack for interpretation. Current measurements may be either single ended, metallic current on either the tip or ring, or differential current on both tip and ring. An analog voltage linearly proportional to the measured current is passed to the fanout with two full-scale sensitivities: ±120 mA and ±80 mA. Digital current thresholds are also available with different sensitivities and different degrees of low-pass filtering.

±10 mA fast (2-ms response)
±10 mA slow (30-ms response)
±10 mA very slow (100-ms response)
−4 mA slow (30-ms response)
−4 mA fast (2-ms response)

Fast-response digital current threshold measurements are used for such functions as power cross detection and ringing current continuity detection. Slow-response thresholds are for such functions as two-party line tip party identification and coin-phone coin-presence tests. Very slow scan points are used for ring-trip.

A high-impedance voltage detector is used to verify connection integrity whenever a metallic access relay on the USC is operated. If another line is connected to this bus inadvertently by control or by a circuit fault, closing another line relay to this bus could result in a short-duration, large current flow, while charge redistribution between the lines takes place. This could damage the dry reed relay that is last to operate. If the detector finds a significant voltage, the function in progress by the USC is halted and attempts are made to clear the unwanted connection before relay damage can occur.

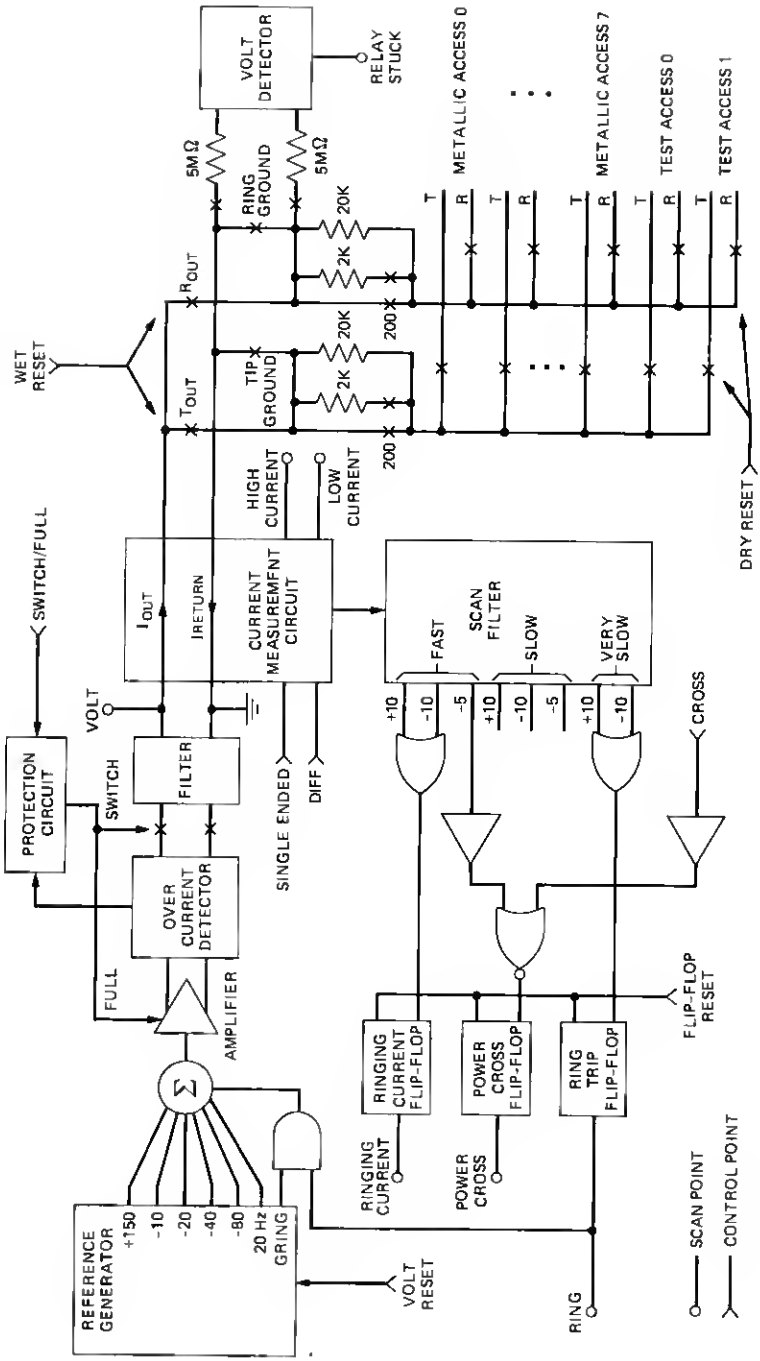


Fig. 16—Universal service circuit block diagram.

4.1.1 The usc voltage source

Figure 17 is a diagram of the USC voltage source. An initial dc-dc switching converter steps up the −48 volt RSS supply voltage to 200 volts. This is followed by the ±125 mA overcurrent detector which shuts down the circuit during overload. The optically coupled bridge switch couples the 200-volt source to the output filter. Depending on the duty cycle of oppositely paired transistors, any voltage up to ±200 volts will be available at the output. The output is heavily filtered with a Balun transformer and capacitance to allow switching mode conversion and eliminate output voltage transients.

To control the bridge switch, a triangular wave is compared to the output of the programmable reference signal generator. One pair or the other pair of transistors in the bridge switch is enabled depending on whether the reference signal is greater or less than the triangular signal. Turn-on delay is added to the control circuitry of the bridge switch to ensure that only one pair is turned on. Otherwise, a short would be placed across the 200-volt supply. The USC voltage source has been described here as a programmable power supply, but it could, just as well, be considered a low-frequency dc-coupled amplifier for the reference signal generator.

4.1.2 The usc current sense circuit

The USC current sense circuit, shown in Fig. 18, uses toroidal ferrite coils to provide isolation from the large voltages present at times on the measured conductors. It is a differential, or metallic, current measurement device as shown, but it is also used as a longitudinal current sensor by bypassing tip or ring current around the device.

The current sense circuit relies on a clock signal to saturate the drive transistor. This provides a current through the drive windings large enough to saturate both toroids and drop their permeability substantially. When the clock signal is removed, the toroids recover from saturation with a large increase in permeability. Any current flow through the tip and ring windings will generate an increase in magnetic field that will induce a current in the sense winding. The sense winding is sampled at this time by a JFET enabled by release of the drive winding, and an inverting integrator begins to supply a current in the sense winding of opposite polarity to that induced by the tip and ring windings. Equilibrium is reached when the integrator provides a current to the sense winding tbat will provide a field exactly opposing that generated by the tip and ring windings. The integrator amplifier output is then a direct function of tip and ring current. Two toroidal cores are used so that the drive signal is canceled in both tip and ring and in the sense windings.

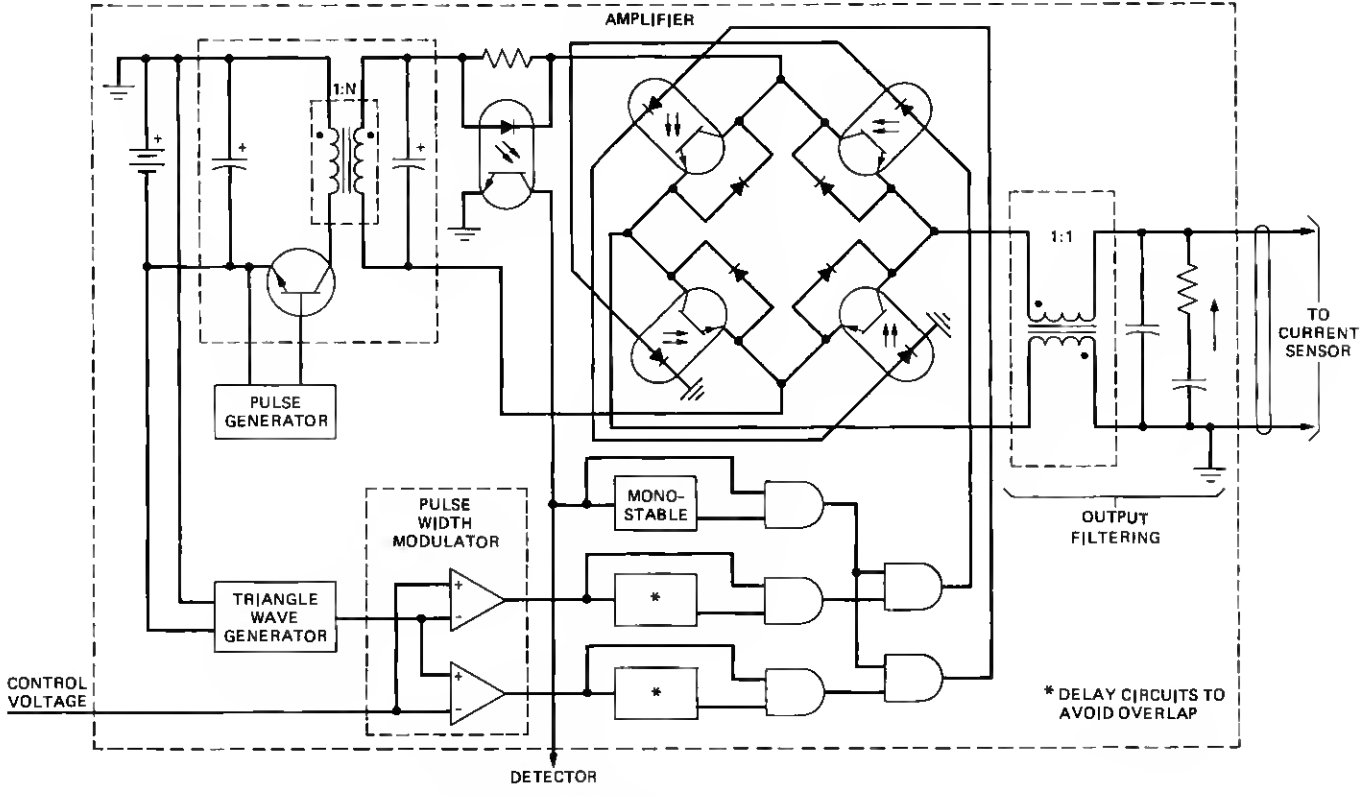


Fig. 17—Universal-level service circuit voltage source.

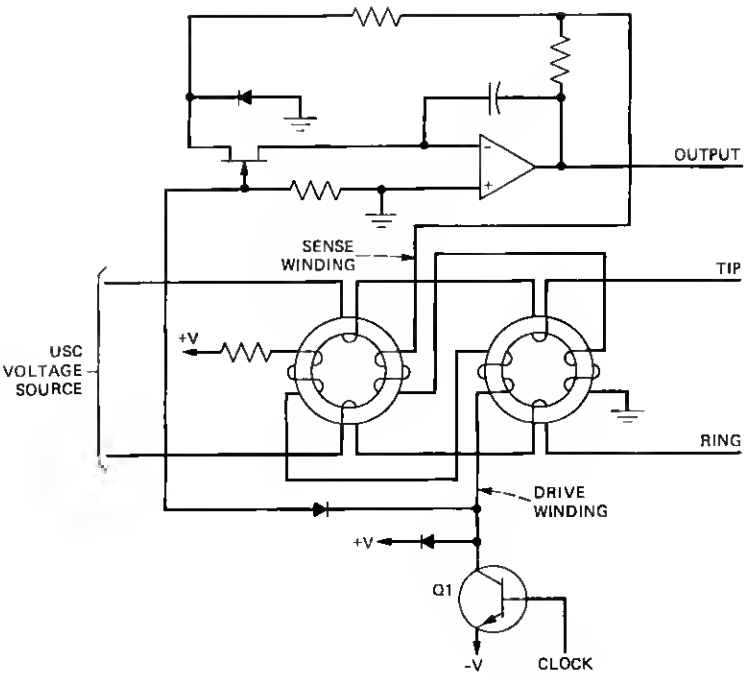


Fig. 18—Universal-level service circuit current sense circuit.

4.2 Metallic access network

The RSS metallic access network is based on a shelf serving 256 lines (Fig. 19). Each line has access to an A and a B bus connecting to two groups of USC circuits. All high-power line functions or test functions requiring metallic dc-coupled line access must use this network. Table II outlines these functions and categorizes them according to actual time required per usage. Because the only function requiring a long holding time was manual loop testing and since this is a very slow occupancy function, the usage of the metallic access network was time-divided.

Figure 20 shows the timing of the metallic access network for one possible very busy bus. In a given bus cycle of 6.9 seconds, three 2-second periods are allowed for functions no longer than 2 seconds. A sample of functions that might occur on a very busy bus is shown. Code-1 ringing (nominally 2 seconds on and 4 seconds off) is easily accomplished with a slight lengthening of the silent interval. The line is supervised by the line circuit during the silent interval before the next ringing interval or ring-trip. Code-2 ringing used for multiparty lines (nominally 1 second on, 1 second off, 1 second on, and 3 seconds off) is compressed to 0.7 seconds on, 0.6 seconds off, 0.7 seconds on

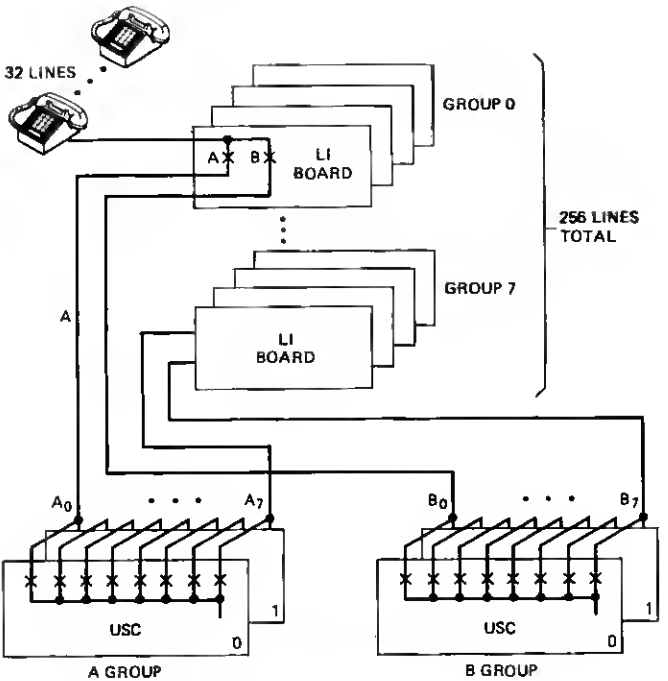


Fig. 19—Metallic access network.

and 5 seconds off. A human factors study of tbe modifications made to code-1 and code-2 patterns was conducted and both codes were found to be satisfactory. The timing of the other functions shown was not affected by time dividing the metallic buses.

With fixed periods for ringing and test functions, the A and B bus groups are run 1.15 seconds out of phase to reduce the average delay of a line receiving metallic bus access. To further reduce delays, test functions will be performed during a bus period if enough time remains

Table II—High-level signaling and testing functions

Holding Time on the Bus		
Short (less than 0.33 s)	Long (less than 2 s)	Continuous
Power cross test*	Single-party ringing‡	Manual loop testing†
Party test*	Multiparty ringing‡	
Coin presence test*	Coin collect or return*	
	Interface circuit testing†	
	Automated loop testing†	

* Low traffic, no delsy scceptable.
† Very low traffic, substantial delsy scceptable.
‡ Repested periodically, high traffic, one period of delay scceptable.

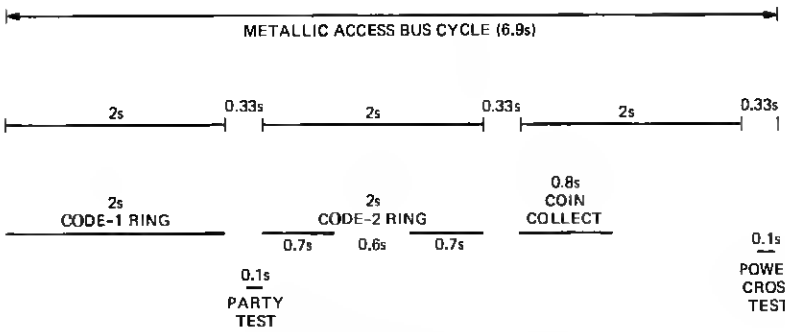


Fig. 20—Metallic access network timing.

even though the period has begun and code-1 ringing will begin if at least half the 2-second interval remains.

Blocking and delay in the metallic access network has been studied with a summary of the results shown in Table III. A bus occupancy corresponding to 0.3 CCS/line was used which is three times the average busy-hour usage expected to allow for peaking. With both buses available, service is excellent with accceptable service still offered during the low-probability period of one bus being out-of-service or used for manual testing. Manual testing is denied to a group of 32 lines that has a bus out of service.

V. CARRIER INTERFACE

All voice connections, supervision, and data between the host ESS and RSS passes over carrier. No provision is available for metallic facilities linking the two since degradations in the audio signal transmission over metallic facilities would be very difficult to overcome.

Two types of carrier interfaces may be provided: a T1 digital carrier interface and an analog carrier interface. The T1 carrier interface is entirely self-contained in the RSS. In many cases, no external T1 carrier

Table III—Metallic access network blocking and delays

	Simultaneous Time Slots		1.15-s Staggered Time Slots	
	Normal	1 Bus Out	Normal	1 Bus Out
Probability delay greater than next time slot	0.005	0.11	0.07	0.11
Probability delay greater than next time slot +1.1 s	—	—	0.005	—
Probability of blocked ringing	$<10^{-7}$	0.0013	$<10^{-7}$	0.0013
Average ringing delay (s)	1.15	1.5	0.68	1.5
Average 2-party dial tone delay (s)	0.06	0.17	0.05	0.17
Probability of blocking a 2-time slot reverting call	10^{-5}	0.034	$<10^{-4}$	0.034

or transmission equipment will be required at the RSS location. In about a third of the RSS applications, however, the use of other carriers is more attractive than T1. This may be because of the reuse of existing equipment or other incompatibilities. In these cases, the analog carrier interface provides a universal 4-wire interface to carrier equipment external to the RSS.

The two carrier interface types may be mixed in a single RSS as groups of 24 channels. Full compatibility is provided in that the two types plug into the same frame locations and are fully control-compatible. Up to 5 of these 24-channel groups may be provided in a single-module 1024-line frame or 10 in a dual-module 2048-line application.

5.1 The RSS T1 carrier interface

The RSS uses 24-channel T1 digital carrier with standard 8-bit μ-255 law Pulse Code Modulation (PCM) voice encoding. A shared coder-decoder (CODEC) is used with a good portion of the circuitry originally developed for the D4 channel bank.[5] Each 24-channel digital group (DIGROUP) is packaged on eight 3/4-inch-spaced circuit packs. Since up to 5 DIGROUPS may be equipped in a single RSS frame, this DIGROUP compactness is a necessity.

Shown in Fig. 21 is a single DIGROUP from RSS to the host ESS. The

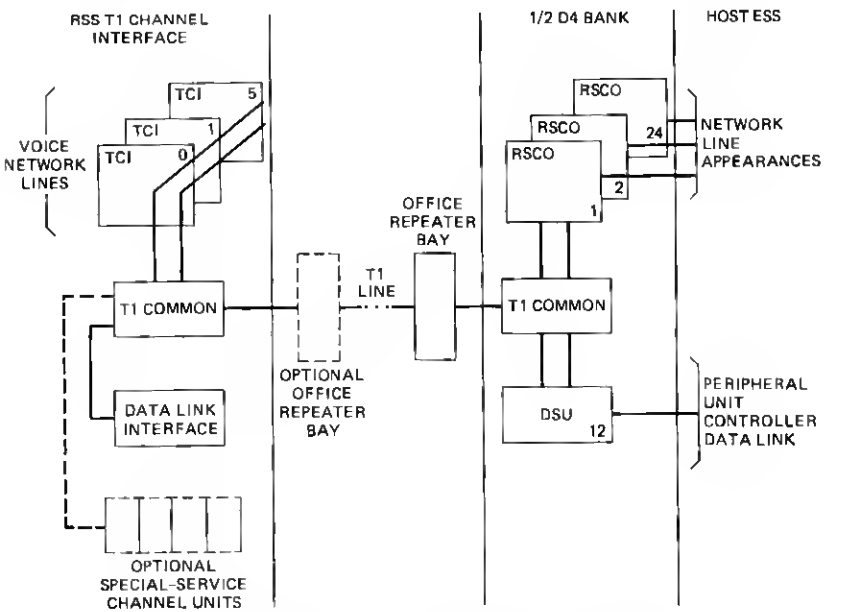


Fig. 21—No. 10A RSS T1 carrier connection for a single DIGROUP.

T-Carrier Interface (TCI) multiplexes up to 24 samples from the voice network links and their associated supervisory state. The T1 common circuitry encodes this information into a 1.554-Mb serial bitstream and drives the two-pair T1 line. Office repeater bays which normally terminate a T1 carrier line are not required at the RSS location if the T1 line span from the last office is not too long to be powered by that office. This distance can be up to 20 miles and will be the normal case when using RSS in a small minihut.

At the host RSS, an office repeater bay is required to interface to the line. A D4 channel bank is then used to decode the T1 signal. A special channel unit called a RSCO (RSS Central Office End) has been designed which has more gain and a different hybrid balance network compared to other standard channel units. Functionally, this unit converts the four-wire transmission of the carrier to the two-wire transmission of the host ESS and provides a supervisory loop closure in the two-wire path. No supervision is detected or transmitted from the host ESS to RSS.

Each of the first two DIGROUPS in RSS also carry a data link, for the control of RSS from the host, and optional special service channels. The data link interface uses channel 12 of each DIGROUP with the TCI disabled for this channel. At the host, a data service unit DSU data port is placed in the D4 bank channel unit position 12 to interface the data channel to the peripheral unit controller data link port of the ESS. As an RSS frame option, cabling may be included to use the last four channels of the first two DIGROUPS for special-service access to the T1 carrier instead of RSS voice channels. In this way, a small number of special services, such as foreign exchange lines, may be provided at an RSS location without having additional carrier equipment. Standard D4 bank channel units are used both in RSS and in the host D4 bank to handle these services.

An RSS T-carrier DIGROUP is shown in Fig. 22. Only three pack codes are used with all the T1 common functions contained on the Transmit-Receive (TR) pack and the Alarm and Line Interface (ALI) pack.

5.1.1 The alarm and line interface

An ALI pack receives the balanced 1.544-Mb T1 line self-clocked bipolar signal. Automatic gain control allows for varying line loss while an inductor-capacitor tank circuit recovers tbe clock and data. This pack must also generate the T1 line signal transmitted from RSS. In this direction, one of several different networks on the pack are enabled with different backplane options on the connector pins. These networks attenuate and shape the line signal when office repeaters are used with RSS and allow for three different cabling distances. The T1 carrier line dc current, used to power line repeaters, may be looped

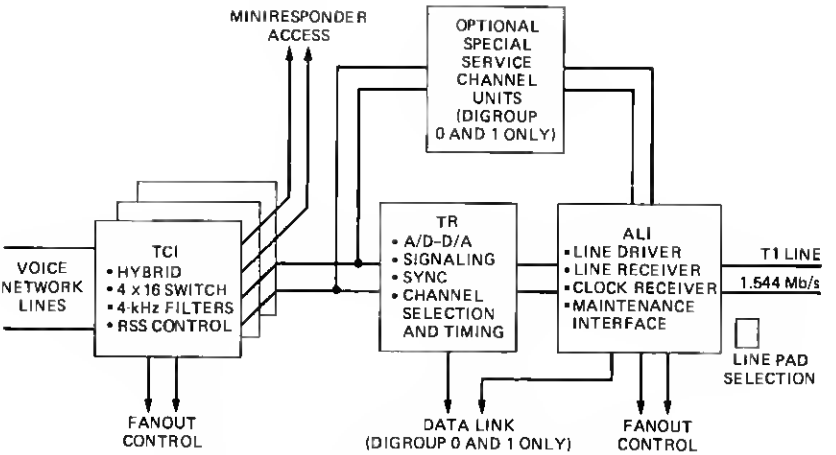


Fig. 22—No. 10A RSS internal T1 carrier interface.

through isolation transformers in the ALI to maintain a sealing current for splices even though no part of the ALI is powered from the T1 line.

Alarm and trunk processing status of the DIGROUP is indicated with LEDs on the ALI. A red alarm from the TR pack, indicating loss of synchronization, is displayed and passed onto control. A yellow alarm, indicating a red alarm at the host for this DIGROUP, is found by integrating a signal from the TR and, if found, it is displayed and also passed to control. If either alarm is found, three relays are operated under program control to trunk process, i.e., place in a benign state, the special-service channel units.

Several clocks which run the DIGROUP are also derived on the ALI. The 1.544-MHz receive clock which is derived from the incoming signal has already been mentioned. A quartz-crystal-based 6.176-MHz clock to run the transmit portion of the TR is synchronized to the receive clock unless a red alarm occurs. Then it is allowed to run free. A third 64-kHz clock for the data link interface and special-service data units is derived from the transmit clock by a phase-locked loop circuit operating from signals from the TR.

5.1.2 The transmit-receive circuit pack

A TR pack contains the shared CODEC and control logic for a DIGROUP. Multiplexed Pulse Amplitude Modulation (PAM) is used to pass samples of the channel audio signals between itself and the TCIs.

The transmit coder performs a sequential sample-and-hold on the PAM sample of each of the possible 24 channels at an 8-kHz rate. This sample is first examined for sign and then a successive approximation analog-to-digital conversion is performed with the comparison level

formed from a thin-film-resistor weighting network. The 8-bit result is serially transferred to the ALI for transmission. In every sixth sample, however, the supervisory state of the channel is also sampled and inserted as the least-significant bit. After all 24 channels have been sampled, a single framing bit is added whose pattern allows the D4 bank receiver to synchronize on the incoming bitstream. If the receive portion of the TR pack is generating an alarm, another bit in each time slot is stuffed to signal the far end with a yellow alarm that a problem exists.

Instead of audio information, each time slot may also contain data. If a TCI does not respond to its enable signals for a time slot, the transmit circuit sends 8 bits of data present on a separate serial data input.

The receive circuit is functionally the inverse of the transmit circuit. Line data with the recovered clock from the ALI pack are examined bit-by-bit for the framing bit, and synchronization is eventually established. If synchronization cannot be established or is broken, an out-of-frame signal to the ALI results in a red alarm. To decode a receive time slot to audio, the 8 bits are directly converted from digital-to-analog using another thin-film weighting network and sent to the TCIs as a PAM sample. At the same time, the proper TCI channel is enabled to receive the sample. In addition, the bit carrying supervision is transferred to the channels every six frames and the bit carrying the yellow alarm is sent to the ALI for yellow-alarm detection.

If data are being sent for a channel instead of an audio sample, no special actions are taken by the receive circuit. The receive bitstream and clock are available to the data link interface pack and special-service channel units to enable extraction of data based on timing from the receive circuit.

5.1.3 The T1 carrier interface pack

The TCI is the first stage of conversion from the RSS voice frequency electronic network and control complex to the T1 carrier line. Each TCI pack provides four audio channels from RSS by including one stage of switching, transmission path conditioning circuitry, and conversion from voice frequency to PAM (Fig. 23). A 16 by 4 PNPN crosspoint switch connects the single transformer hybrid circuit of a channel into the voice network. The hybrid balancing network contains an inductor to balance out the shunt inductance of the hybrid itself and the line circuit transformer. To balance the line impedance, two different networks previously selected by the electronic line segregation circuit are used. In the four-wire portion of the circuit following the hybrid, 2 dB of loss may be added. This loss is inserted on short loops where *TOUCH-TONE* service signals may be clipped by the PCM encoding

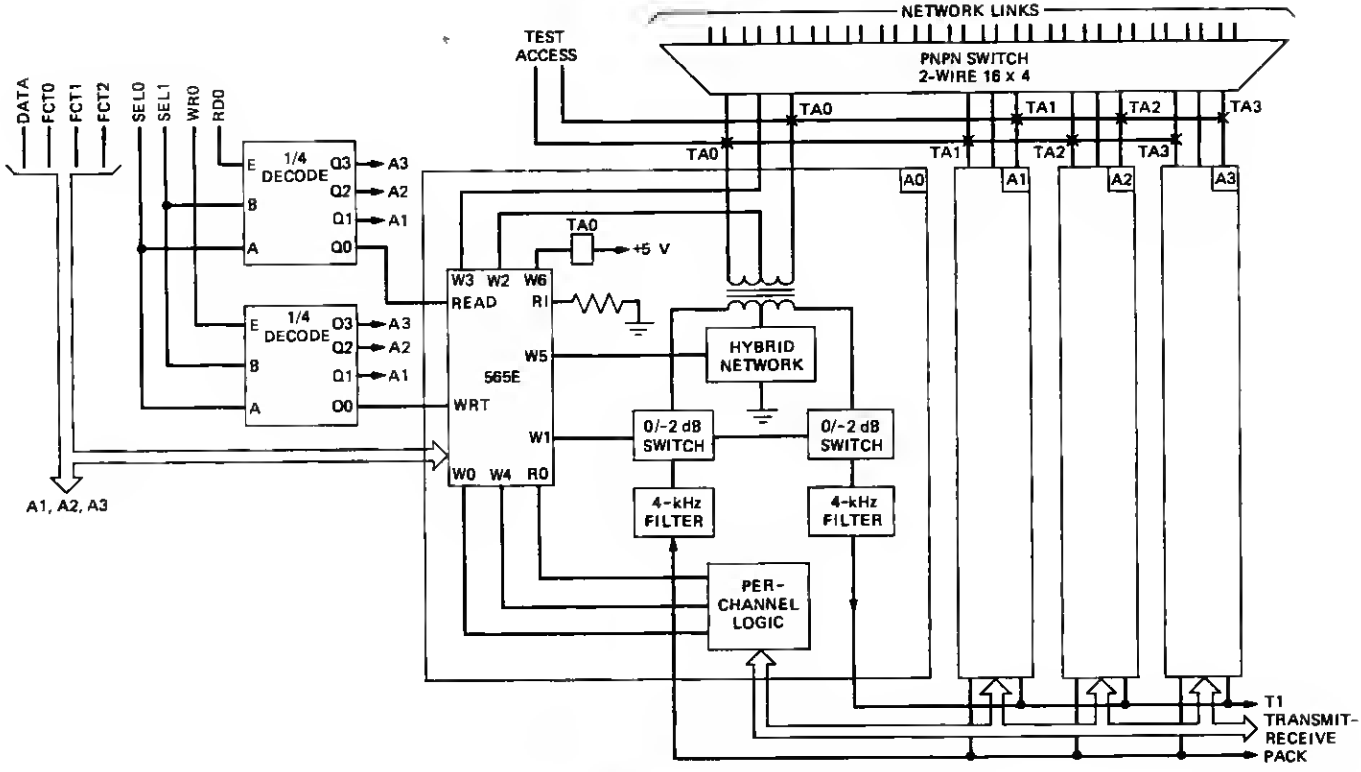


Fig. 23—No. 10A RSS T1 carrier interface circuit pack.

or if a line is suspected of being an extremely poor impedance match to the balancing networks. After this, 4-kHz cutoff low-pass filters prevent aliasing and noise from the PAM signals. A 60-Hz notch filter is included in the transmit filter. Per-channel logic interprets the timing signals from the TR pack. This logic controls PAM bus and supervision bus usage.

The same custom IC used per line circuit controls each channel. Network control is identical, with the other functions unique: a test access relay may be operated to allow miniresponder access for transmission testing, the hybrid network state, 2-dB loss, receive supervision for test purpose only, transmit supervision, and channel receive PAM bus enabling. This last function is used to stop audio reception when the channel is not in use to eliminate a possible oscillation condition and to quiet the channel when an alarm is present. Again, the state of the latches in this circuit may be interrogated under fanout pack control.

5.2 The analog carrier interface

When other carriers besides T1 using D4 banks are used with RSS, the carrier equipment is external to the RSS frame (Fig. 24). The data links are interfaced to the carrier using modems. A new interface for the audio channels is now also required between the RSS and its carrier terminal and between the carrier terminal at the host ESS and its network.

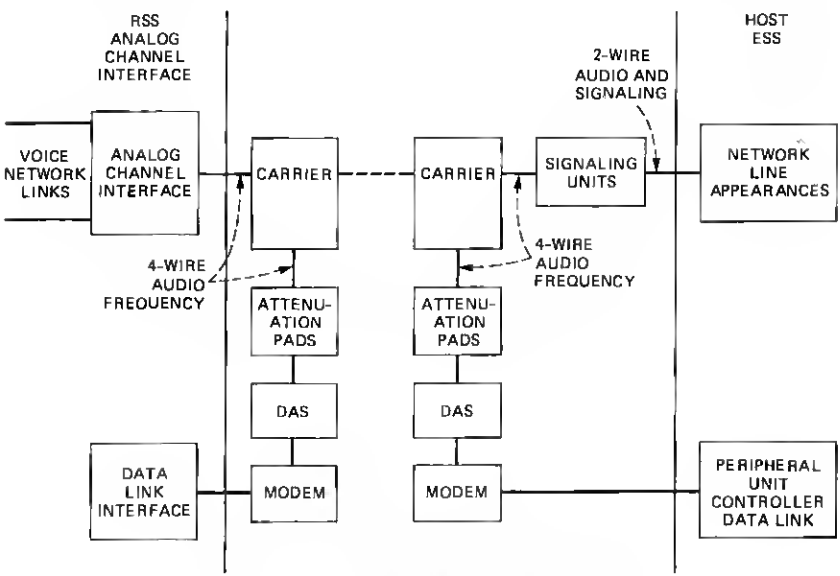


Fig. 24—No. 10A RSS general carrier interface.

At RSS, the Analog Carrier Interface pack (ACI) provides conversion from the RSS two-wire transmission voice frequency electronic network and the control complex to the four-wire transmission and Single Frequency (SF) signaling used by the carriers. As may be seen in Fig. 25, the ACI is identical to the TCI in RSS control and until after the 2-dB loss section of the four-wire transmission path. This similarity is important as it maintains control compatibility between the two. The difference after this point is due to the four-wire audio connection to the carrier and SF signaling.

Each ACI pack has a quartz-crystal-based 2600 Hz sine wave generator, with a voltage reference controlled output level as a source for SF signaling tone. Each channel contains a timing IC for signaling that also uses the 2600 Hz as a time base. When the channel is on-hook, −36 dBm 0 SF is transmitted and the audio from the hybrid is cut off. When the channel goes off-hook, SF is cut off and the hybrid audio is cut through after 120 ms delay. If the channel goes back on-hook, audio is immediately cut and −24 dBm 0 SF is transmitted for 400 ms. If the channel is still on-hook after 400 ms, the SF is reduced back to −36 dBm 0.

An audio cut-off under individual control is in the receive path to emulate the receive PAM bus enabling control available on a TCI channel. An adjustable attenuator with a range of 1.5 dB is included in both transmission directions of an ACI channel to allow for wiring losses to the carrier bank.

At the host ESS (Fig. 24), an SF unit, including the special balancing network for the four-wire to two-wire hybrid, was made by adding a slight modification to an already existing SF signaling unit.

VI. TEST CIRCUITS

Two families of test circuits exist in the RSS. Some circuits are used to test customers' telephone lines, while the rest are part of transmission testing.

Line testing equipment is designed to be compatible with existing test facilities like the Local Test Desk (LTD). Craft are able to remotely test RSS lines with the same ease that they test host lines.

Transmission testing equipment is also designed to be compatible with existing test facilities. Automatic testing of the transmission facilities between the RSS and host is accomplished by circuits similar to those in No. 1 ESS type trunk testing equipment.

6.1 Line testing

Customer line testing is done through the ringing bus of the RSS. A Test Access Bus (TAB) runs between all Universal Service Circuits (USCs) and to all line testing circuits. The USC is able to connect the

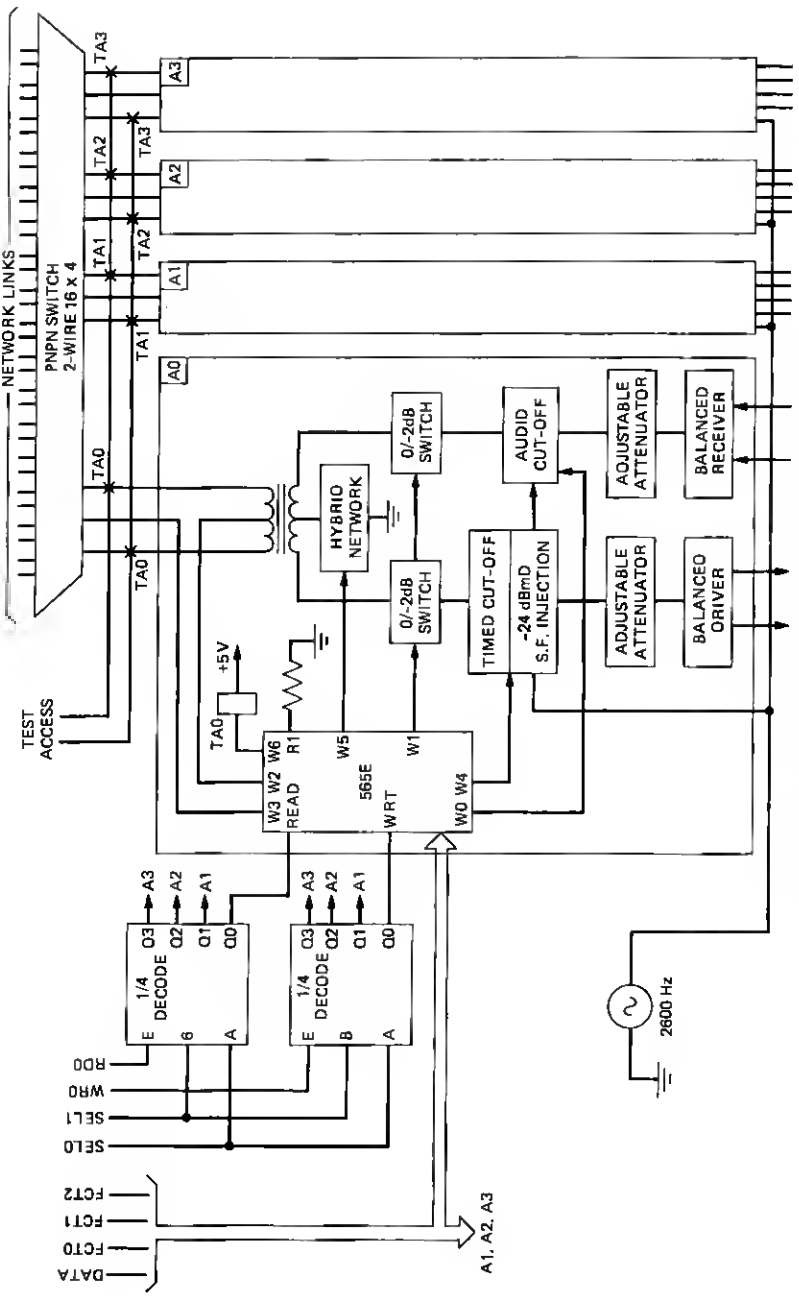


Fig. 25—No. 10A RSS analog carrier interface circuit pack.

TAB to one of its ringing buses. A test circuit reaches a line by seizing the TAB, an idle USC, and one of the ringing buses.

If the 10A RSS is within metallic range of the LTD, a pair of wires is run from the host to the RSS (see Fig. 26). The LTD connects to the host in the usual manner through an LTD trunk.

The metallic test path terminates as a line appearance on the host. Out at the RSS, the loop terminates on a pair of boards called Metallic Line Access Ports (MLAP). Under control of the host, they provide the connection from the test path to the TAB.

For those cases where the RSS is too far from the host, telemetry is used. This telemetry system is an option on the LTD. The corresponding remote line testing equipment is available for use by all switching systems. The Remote Line Test (RLT) equipment for RSS is functionally the same as for other systems, only the implementation is different (see Fig. 27). Three boards have replaced half of a frame of equipment.

In Fig. 27, note the circuit at the interface between LTD and LTD trunk. This circuit, called the Local Test Desk Applique (LTDA) monitors all signals sent to the RLT. When a code is seen from the desk that requires action by the host, the LTDA passes the data to the LTD trunk. By injecting data at this point in the system, much of the existing line testing software was utilized.

Line testing through an RSS has one major problem not found in other ESSs. Each line on the RSS has a pair of resistors associated with it to bias the line negative. A 100-kilohm resistor is present from the tip to a −96 volt supply. The ring conductor has similar treatment. If unassisted test equipment tried to read leakage or foreign potentials on the customer's line, the 100 kilohms and −96 volts would be seen.

This problem is solved by using precision negative 100-kilohm resistors tied to −96 volts during line testing (see Fig. 28). The parallel combination of the positive and negative resistors is nominally an open circuit. Under worst-case conditions, the magnitudes of the 100-kilohm bias resistors are still boosted to a value over 8 megohms.

One negative 100-kilohm resistor exists on each MLAP board. The

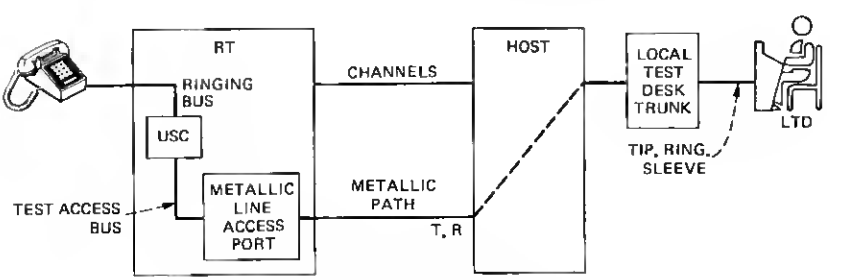


Fig. 26—Line test equipment using a metallic test path.

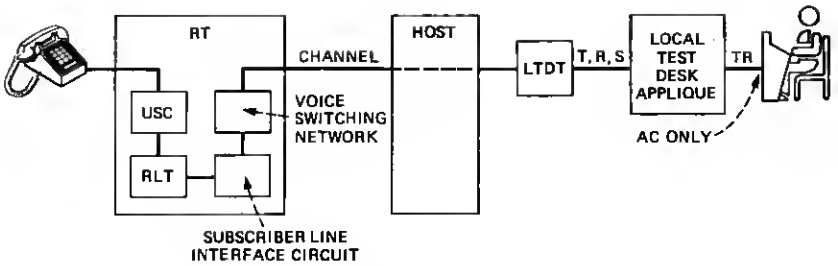


Fig. 27—Line test equipment using a telemetry path.

complexity of this board comes from two requirements. First, the worst-case tolerance of the negative resistor must be better tban ±0.2 percent. Secondly, it must keep that accuracy over an applied voltage range of −96 volts to +200 volts. This voltage range is necessary to prevent any line testing equipment from saturating the negative resistor circuits and seeing the 100-kilohm resistors.

A number of circuit techniques are employed to meet the above requirements. A structure was chosen that contains a Multiplying Digital-to-Analog Converter (MDAC). With it circuit gain can be adjusted until the negative resistor has the proper value. The MDAC is controlled by a calibration circuit that also resides on the board. The calibration circuit contains a precise positive 100-kilohm resistor which can indicate when negative 100 kilohms has been achieved.

Linearity of the negative resistor is essential to the overall circuitry accuracy. A low-cost MDAC with the same linearity as an operational amplifier was developed. Speed is not important here so miniature mercury relays are used to switch various resistors into the signal path.

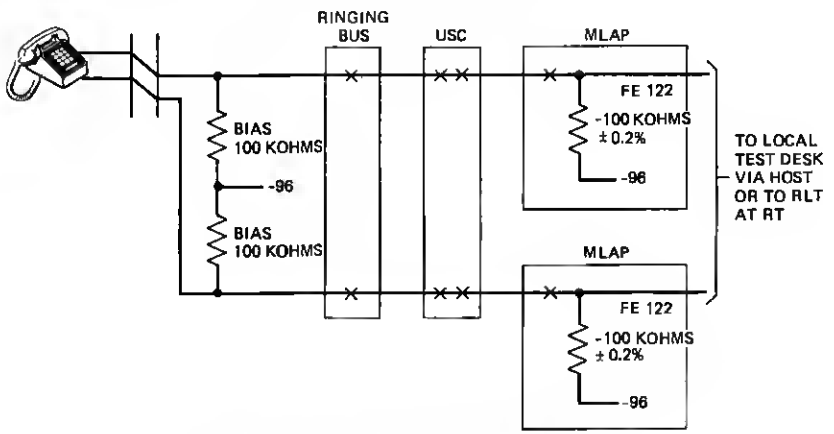


Fig. 28—Line testing with bias resistors.

The result is a very linear 8-bit MDAC with a large dynamic range passing through 0 volts.

Another source of potential nonlinearity is the transistor operated as a currrent source. We have two current sources in the signal path. They must have a large dynamic range and a constant gain. The alpha of the output transistors is a function of collector current and, therefore, was a potential problem.

The problem was solved by using local feedback. Any transistor with a beta greater than one becomes able to have an effective alpha very close to one. In practice, no variation in alpha can be seen over four decades of collector current.

The large voltage range of the negative resistor requires high-voltage transistors. When worst-case parameters are considered, little margin for transients exists. Rather than use even higher voltage transistors, a new circuit was developed. We have available a signal proportional to the collector voltage of our critical transistor. This information is used to quickly move the emitter of that same transistor. In this way, the collector-to-emitter voltage can be set to a single value independent of the collector voltage. Part of a quad operational amplifier and a small floating power supply are required. A low-voltage transistor can then stand a large voltage on its collector.

6.2 Transmission testing

Most of the transmission test equipment in the RSS resides on one board. This board includes an automated transmission test circuit called the miniresponder in addition to a number of tone sources and a tone detector. A microprocessor on the board is used for local control.

The miniresponder is functionally the same as a 56A remote office test line. It operates under the control of the CAROT to test carrier channels between the RSS and host.

During a transmission test, the CAROT transmits multifrequency signals to the miniresponder over the path to be tested (see Fig. 29). In response, the miniresponder configures itself to do the test. Then it either sends or receives test tones and, if required, reports the results to CAROT.

Upon command, the miniresponder can do various two-way loss and noise tests. If the microprocessor detects a problem in the miniresponder, it can give a detailed account to CAROT.

The tone sources available on this board are used for manual testing of carrier channels. Requests for a tone source can be initiated from one of the host's maintenance trunk test panels. This causes a data link message to be sent to the RSS which, in turn, instructs the board to output the proper signal. Circuit failures are detected by the on-board microprocessor and passed back to the RSS. A data link message is then sent to the craft indicating the problem.

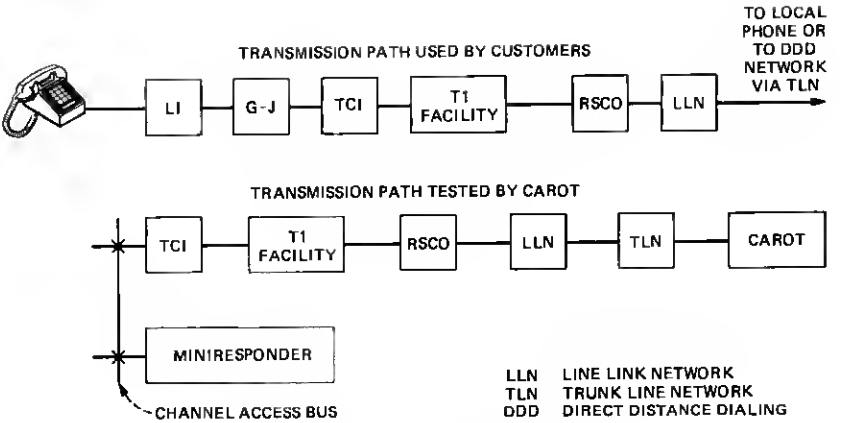


Fig. 29—Transmission testing.

Up to this point transmission testing of carrier channels has been considered. Alternating current testing is also done within the RSS. This is to ensure that customers have ac continuity through the line appearances to the network. As part of the line interface diagnostic, a tone is applied to the customer's line via the TAB. It is seen by a tone detector switched to that line appearance through the network.

VII. LOW-LEVEL SERVICE CIRCUITS

7.1 Functions

Normally, tones such as dial tone, busy, reorder, and audible ring are supplied by the host ESS and sent to an off-hook customer over one of the available voice channels. *TOUCH-TONE* service digits from a customer *TOUCH-TONE* pad are also received and decoded by the host ESS using one of its *TOUCH-TONE* service receivers. However, when the RSS is in stand-alone, because of the loss of both data links, the host facilities cannot be used and these functions must be provided within the RSS frame.

The ROH tone is never sent from the host ESS to an off-hook customer. The high level of this signal would overload the corresponding T1 Carrier Channel resulting in the ROH signal being distorted. The ROH tone is, therefore, also generated within the RSS frame.

A general-purpose ac source and matching ac detector are provided within the RSS frame for performing ac continuity tests on network A-links, junctors, and line circuits.

7.2 Circuits

The *TOUCH-TONE* service circuit pack contains the precise tone plant and *TOUCH-TONE* service receiver circuit. The precise tone

plant produces dial tone, busy tone, reorder tone, and audible ring. Circuitry is also provided to interface a recorded announcement machine into the RSS network. The circuit pack also contains an 8 by 16 first-stage switch that provides 8 appearances to the network. Up to six TT circuit packs are used in a frame with the number being dependent on frame line size.

The ROH/ELS circuit pack contains the ROH tone source and detector, a 1400-Hz test source, an ac continuity detector, and the Electronic Loop Segregator (ELS). The ELS portion will be described elsewhere. The circuit pack also contains an 8 by 16 first-stage switch that provides 8 appearances to the network. The ac continuity detector also has a metallic test-access bus appearance for use in performing ac continuity tests of line interface circuits. There is one ROH/ELS circuit pack per RSS frame.

VIII. POWER

The RSS frame uses a single battery voltage of −48 volts, making it compatible with existing CDO battery plants. It has a current drain of up to 20 amps depending upon frame circuit pack equipage and active call traffic.

Besides −48 volts, within the RSS frame, there exists a multiconverter complex to provide five additional voltages of +5, +12, +24, −12, and −96, as needed by the electronic circuitry used throughout the frame.

8.1 Converters

As shown in Figs. 30 and 31, the RSS power complex uses various types of power converters. Some of the converters are dedicated to a certain group of packs, while others are connected in a parallel fashion on a common bus, which is then used throughout the entire frame. Also, some of the converters have a single output voltage, while others are of the multivoltage type—all converters used are of the pulse width controlled (PWC) type.

The power complex has been designed around a modular philosophy in that all converters are pluggable and all are *not* needed in the basic frame configurations. Hence, the power complex grows with the number of lines and channels.

8.2 Distribution

The philosophy behind distribution of power to and within the RSS frame is consistent with that philosophy used in all other areas of the frame design: there should be *no* single fault which would eliminate service to more than 64 customer lines. This has been accomplished by the following (refer to Fig. 30.):

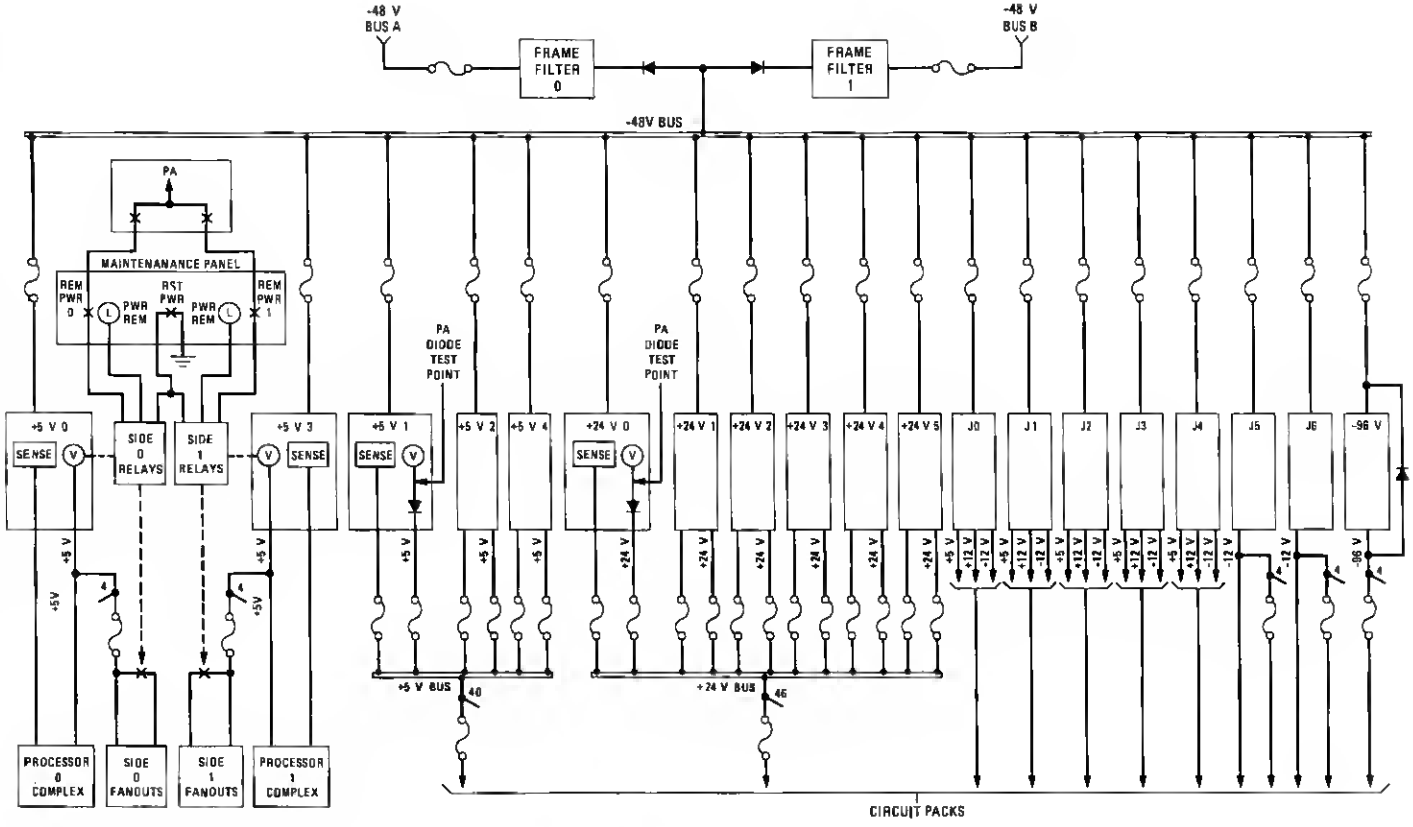
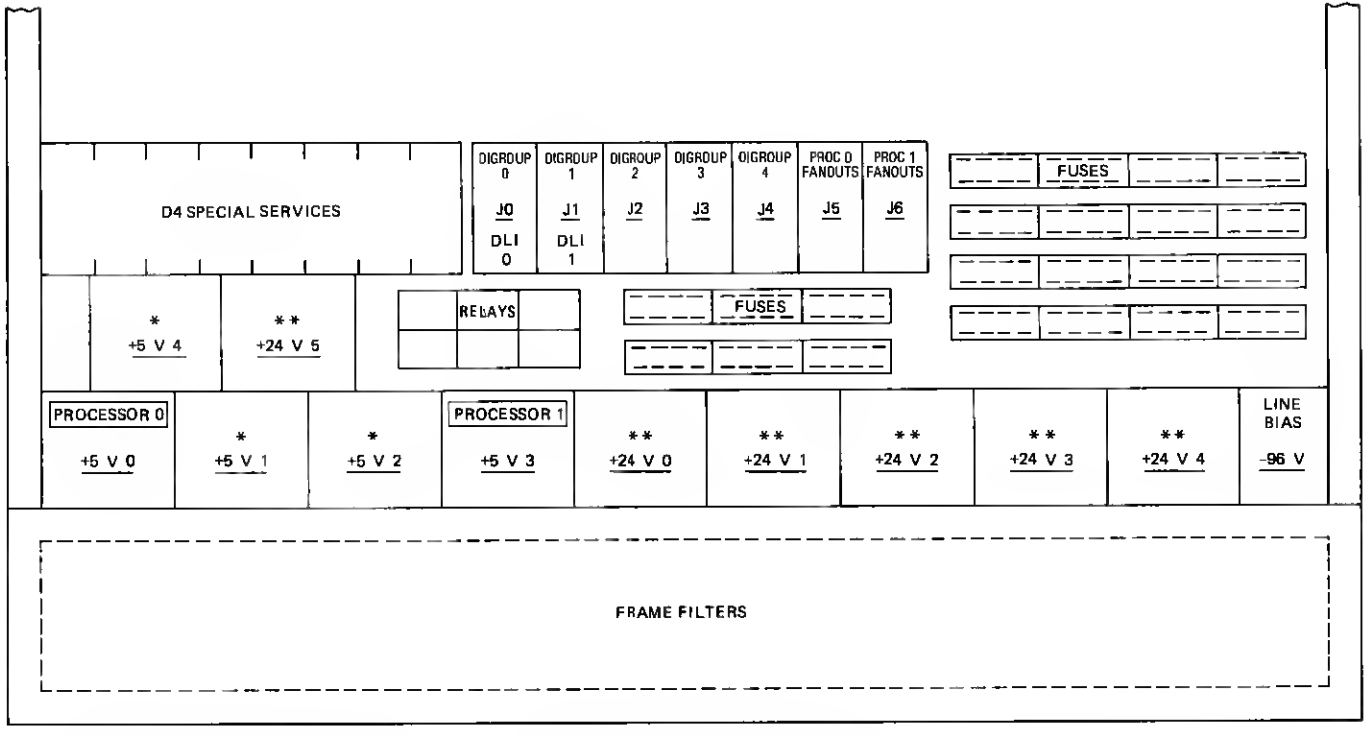


Fig. 30—Power distribution.



* CONVERTERS +5 V 1, 2, 4 ARE CONNECTED IN PARALLEL TO A COMMON +5 V BUS.

** CONVERTERS +24 V 0-5 ARE CONNECTED IN PARALLEL TO A COMMON +24 V BUS.

Fig. 31—Converter identification.

(*i*) Circuit packs have been fused such that any blown fuse will not cause a service outage to more than 64 lines (180 fuses total).

(*ii*) The main −48 volt frame power bus has been duplicated from the battery plant and connected together at the RSS in a "diode OR" manner before powering the frame.

(*iii*) The dedicated power converters have only been used on those circuits which are duplicated or nonservice affecting (microprocessor, DIGROUPS, DLI, miniresponder, RLT, ROH/ELS).

(*iv*) Two groups of converters in the power complex have been connected in the aforementioned parallel manner on a common bus in order to provide two very reliable system voltages of +5 and +24 volts. The number of converters used within each group is based on frame load (circuit pack equipage) and an $n + 1$ philosophy to provide an on-line hot spare. As shown in Fig. 30, each converter within a group is also connected to its common bus through an "ORing diode" for system protection and isolation against a converter fault.

8.3 Monitoring

The various power complex functions (converter output voltages, fuse alarms) are monitored by the RSS processor using the power alarm monitor (PA) circuit pack.

The 180 fuses in the power complex have been logically divided into 19 groups. Associated with a fuse group is a scan point on the PA. When a fuse blows, the corresponding group scan point is activated on the PA to indicate a blown fuse condition to the processor. The determination of which exact fuse is blown is left up to central office personnel by the visual indication presented on the fuse block near the base of the frame. (There is a separate visual indicator per fuse.)

Each voltage produced by a power converter in Fig. 31 has a corresponding scan point associated with it on the PA, resulting in 29 different converter scan points. The processor can monitor the condition of the power converters by determining if these scan points are within a specific range.

8.4 Diagnostics

Several diagnostic features have been designed into the power complex to maintain its integrity.

A diagnostic feature has been provided on the PA to ensure that there are no fuse alarm scan points stuck in a normal state and not capable of indicating a fuse alarm. By operating a distribute point on the PA, all fuse alarm scan points will toggle to the alarm state.

Those converters which are connected to a common bus must be routinely tested to ensure that their ORing diodes are not shorted and will perform their duty in the event of a converter fault. The RSS

processor via the PA routinely shuts down each paralleled converter, one at a time, and measures the corresponding converter output voltage on the converter side of the ORing diode. (Refer to Fig. 30.) If the ORing diode is not shorted, the output will decay to 0 volts. Several hardware safeguards have been designed into the converter shutdown circuitry on the PA to prevent an RSS processor from maliciously or accidentally shutting down a power converter. Also, once a converter has been shutdown, hardware prevents another shutdown until the first converter is restored to service.

The PA has also been designed such that any single hardware failure on the circuit pack will not affect the power converters in such a way that overall system service is affected.

IX. SUMMARY

Various circuits have been described here in the areas of line interface, transmission, line testing, and power.

A 10A RSS customer's line is powered and supervised by an efficient switching-mode battery feed circuit. The customer receives ringing and other high-voltage signals from a universal-level service circuit which gains access to the line through a time-shared relay access network. Audio from the customer is switched through a low-level integrated electronic network to either another customer or to a carrier channel back to the host ESS. Two types of carrier interfaces may be used, self-contained T1 carrier, or a general interface to external carrier banks.

Testing of customer lines is done with LTD compatible equipment. Both metallic and remote testing is possible.

All transmission tests use a single circuit pack. Using a microprocessor, it is able to communicate with automatic, as well as manual, test equipment at the host.

REFERENCES

1. USITA Equipment Compatibility Committee. Minutes of USITA—ATT Meeting, October 4 and 5, 1978, Washington, D.C.
2. P. W. Shackle et al., "A Low Substrait Leakage Junction Isolated P-N-P-N Crosspoint Array," IEEE J. of Solid-State Circuits, *SC-13*, No. 2 (April 1978), pp. 210–18.
3. P. C. Davis, J. F. Graczyk, and W. A. Griffin, "Design of an Integrated Circuit for the T1C Low-Power Line Repeater," IEEE J. of Solid-State Circuits, *SC-14*, No. 1 (February 1979) pp. 109–20.
4. A. A. Yiannolios, "Buried Injector Logic: Second Generation I^2L Performance," IEEE Solid-State Circuits Conf. Digest of Technical Papers, *21* (1978), pp. 12–3.
5. W. G. Albert et al., "D4: Up-To-Date Channel Bank for Digital Transmission Plant," Bell Laboratories Record, *55*, No. 3 (March 1977), pp. 66–72.